CLAIMS

What is claimed is:

1. A frequency doubler device comprising:

a first rectifier doubler stage adapted to receive a first input signal having a first frequency and adapted to output a first rectified signal having multiple harmonics;

a second rectifier doubler stage adapted to receive a second input signal having the first frequency and offset in phase from the first input signal and adapted to output a second rectified signal, wherein the second rectified signal has the multiple harmonics and is offset in phase from the first rectified signal; and

a differential amplifier stage coupled to the first rectifier doubler stage and the second rectifier doubler stage and adapted to sum the first rectified signal and the second rectified signal to produce an output signal, wherein the output signal includes a desired output harmonic having a frequency that is double the first frequency, wherein the summing results in the substantial cancellation of unwanted output harmonics in the output signal.

2. The device of claim 1 wherein the output signal includes even output harmonics and odd output harmonics, wherein the summing results in the substantial cancellation of the even output harmonics in the output signal.

3. The device of claim 2 wherein the even output harmonics are reduced at least 20 dBc relative to the desired output harmonic.

4. The device of claim 2 wherein a first even output harmonic is reduced at least 20 dBc relative to the desired output harmonic.

5. The device of claim 1 wherein summing of the differential amplifier stage results in at least a 20 dBc reduction of an unwanted output harmonic relative to the desired output harmonic of the output signal.

6. The device of claim 1 wherein summing of the differential amplifier stage results in at least a 40 dBc reduction of an unwanted output harmonic relative to the desired output harmonic of the output signal.

7. The device of claim 1 further comprising:

a polyphase network adapted to receive a signal having the first frequency and output the first input signal and the second input signal.

8. The device of claim 1 wherein the second input signal is offset in phase by approximately 90 degrees from the first input signal.

9. The device of claim 1 wherein the differential amplifier stage comprises a first transistor and a second transistor, the first rectified signal coupled to a base of the first transistor, the second rectified signal coupled to a base of the second transistor.

10. The device of claim 9 wherein the output signal is taken across collector terminals of the first transistor and the second transistor.

11. The device of claim 1 further comprising an integrated circuit device, the first rectifier doubler stage, the second rectifier doubler stage and the differential amplifier stage implemented within the integrated circuit device.

12. A frequency multiplier device comprising:

a first rectifier stage adapted to receive a first input signal having a first frequency and adapted to output a first rectified signal having multiple harmonics;

a second rectifier stage adapted to receive a second input signal having the first frequency and offset in phase from the first input signal and adapted to output a second rectified signal, wherein the second rectified signal has the multiple harmonics and is offset in phase from the first rectified signal; and

a differential amplifier stage coupled to the first rectifier stage and the second rectifier stage and adapted to sum the first rectified signal and the second rectified signal to produce an output signal, wherein the output signal includes a desired output harmonic having a frequency that is a multiple of the first frequency, wherein the summing results in the substantially cancellation of unwanted output harmonics in the output signal.

13. The device of claim 12 further comprising:

a polyphase network adapted to receive a signal having the first frequency and output the first input signal and the second input signal.

14. The device of claim 12 wherein the second input signal is offset in phase by approximately 90 degrees from the first input signal.

15. The device of claim 12 wherein summing of the differential amplifier stage results in at least a 20 dBc reduction of an unwanted output harmonic relative to the desired output harmonic of the output signal.

16. The device of claim 12 wherein summing of the differential amplifier stage results in at least a 40 dBc reduction of an unwanted output harmonic relative to the desired output harmonic of the output signal.

17. The device of claim 12 wherein the first rectifier stage comprises a first rectifier doubler stage and the second rectifier stage comprises a second rectifier doubler stage;

wherein the output signal includes the desired output harmonic having a frequency that is double the first frequency.

18. The device of claim 12 further comprising an integrated circuit device, the first rectifier stage, the second rectifier stage and the differential amplifier stage implemented within the integrated circuit device

19. A method of frequency multiplication comprising the steps of:

doubling a first input signal having a first frequency to produce a first doubled signal having a second frequency and multiple harmonics, the second frequency approximately twice the first frequency;

doubling a second input signal having the first frequency and offset in phase from the first input signal to produce a second doubled signal, wherein the second doubled signal has the second frequency and the multiple harmonics and is offset in phase from the first doubled signal; and

summing the first doubled signal and the second doubled signal to produce an output signal including a desired output harmonic having the second frequency, wherein the summing results in the substantial cancellation of unwanted output harmonics in the output signal.

20. The method of claim 19 wherein the output signal includes even output harmonics and odd output harmonics, wherein the summing results in the substantial cancellation of the even output harmonics in the output signal.

21. The method of claim 20 wherein the summing results in at least a 20 dBc reduction of the even output harmonics relative to the desired output harmonic.

22. The method of claim 19 wherein the summing results in at least a 20 dBc reduction of a first even output harmonic relative to the desired output harmonic.

23. The method of Claim 19 wherein summing results in at least a 20 dBc reduction of an unwanted output harmonic relative to the desired output harmonic.

24. The method of Claim 19 wherein summing results in at least a 40 dBc reduction of an unwanted output harmonic relative to the desired output harmonic.

25. The method of Claim 19 further comprising:

receiving a signal having the first frequency; and

generating the first input signal and the second input signal from the signal, wherein the second input signal is offset in phase from the first input signal.

26. The method of Claim 19 wherein the second input signal is offset in phase by approximately 90 degrees from the first input signal.

27. The method of Claim 19 wherein the summing comprises summing the first doubled signal and the second doubled signal by:

coupling the first doubled signal to a base of a first transistor of a differential amplifier;

coupling the second doubled signal to a base of a second

transistor of the differential amplifier; and

taking the output of collectors of the first transistor and the second transistor to form the output signal.

28. The method of Claim 19 wherein the doubling steps comprise:

inputting the first input signal to a first rectifier doubler stage to produce the first doubled signal; and

inputting the second input signal to a second rectifier doubler stage to produce the second doubled signal.

29. A method of frequency multiplication comprising the steps of:

multiplying a first input signal having a first frequency to produce a first multiplied signal having a second frequency and multiple harmonics, the second frequency a multiple of the first frequency;

multiplying a second input signal having the first frequency and offset in phase from the first input signal to produce a second multiplied signal, wherein the second multiplied signal has the second frequency and the multiple harmonics and is offset in phase from the first multiplied signal; and

summing the first multiplied signal and the second multiplied signal to produce an output signal including a desired output harmonic having the second frequency, wherein the summing results in the substantial cancellation of unwanted output harmonics in the output signal.